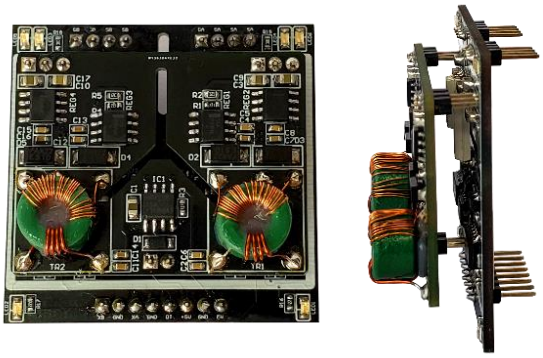
DRVM02
Insulated Dual Gate Driver



Description

The DRVM02 is a dual insulated Gate Driver designed for Si MOSFET/IGBT devices up to 650 V operating in ‘leg configuration’. It is suitable for driving MOSFETs/IGBTs with large input capacitance operating at high frequencies. The compact design of DRVM02 (46 x 47 x 21 mm) enables a very small footprint for high power density applications. It also has selectable shoot-through protection with an intrinsic dead time.

Features

- +14.6 V / -5.0 V output voltage for high/low output signals
- 3 A of sink/source output current
- 0.25 W of output power

Applications

- DC to DC Switch-Mode Power Supplies
- AC to DC Switch-Mode Power Supplies
- Solar Microinverters
- Solenoid and Motor Drives

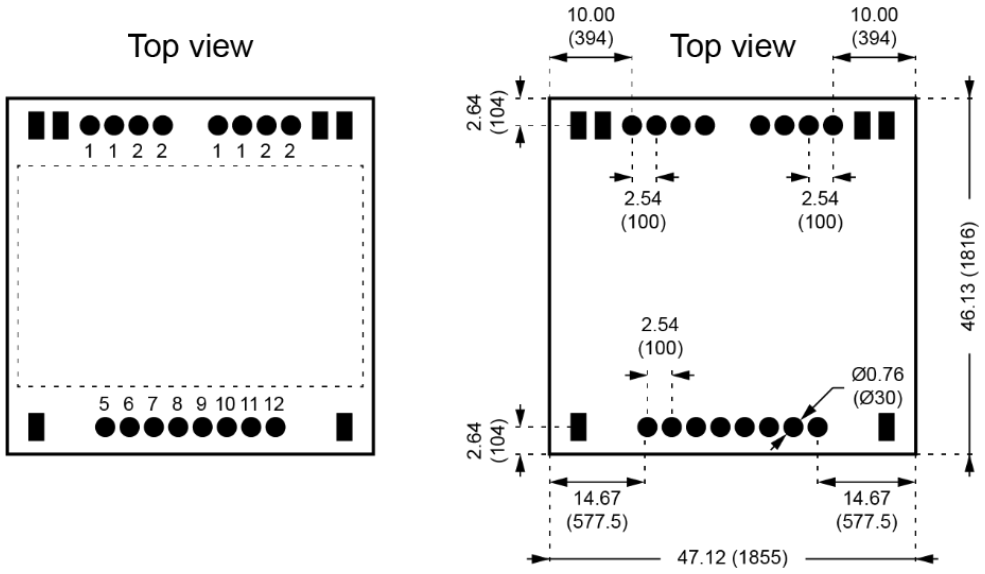
Pin Configuration and Functions

Table 1 – Pin description

Pin No.	Symbol	Description
1	GB	Gate output signal related to channel B. Must be connected to the Gate pin of the MOSFET/IGBT
2	SB	Source output signal related to channel B. Must be connected to the Source pin of the MOSFET/IGBT
3	GA	Gate output signal related to channel A. Must be connected to the Gate pin of the MOSFET/IGBT
4	SA	Source output signal related to channel A. Must be connected to the Source pin of the MOSFET/IGBT
5	XB	PWM input signal related to the channel B
7	XA	PWM input signal related to the channel A
9	DT	Shoot-through protection pin. If connected to GND or left floating, the shoot-through protection is activated and no high-level gate signals are transferred to the driver outputs at the same time. The activation of this protection also impose a minimum dead-time between the two channels (250 ns). To deactivate the shoot-through protection this pin must be connected to 3.3 V (max)
10	VCC	Power supply pin. Must be connected to +5.0 V
6,8,11	GND	Power supply/input PWM signal reference
12	EN	This pin must be connected to GND

Package Outline

Units: mm (mil)



Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
Supply voltage	4.75	5	5.25	V
PWM pin input voltage	3	-	3.3	V
Shoot-through protection pin input voltage	3	-	3.3	V
Delay time	-	-	150	ns
Common Mode Transient Immunity	35	50	-	kV/µs
Pulse Width Distortion	-	-	65	ns
Insulation Voltage (DC)	2.5	-	-	kV
Output Power	-	-	0.25	W
High Level Output Voltage (1)	-	14.6	-	V
Low Level Output Voltage (1)	-	-5	-	V
Maximum Output Current (2)	-	-	3	A
Dead time (3)	-	250	-	ns
External gate resistor	5.6	-	-	Ω

Notes:
(1) Series resistive-capacitive load (R = 5.6 Ω/C = 10 nF)
(2) Minimum recommended external gate resistor (R = 5.6 Ω)
(3) With shoot-through protection activated

Layout Guidelines

To achieve a well-behaved gate signal, the distance between the gate driver and the MOSFET/IGBT should not be larger than 15 mm (even without using super junction devices). If the distance is larger than 15 mm, gate signal oscillations could impose a wrong commutation, possibly causing a component/circuit failure. The signal area containing the controller/conditioning circuitry must be separated from the high voltage/current area, and power and signal tracks should never cross each other, even if they are in different PCB layers.

The minimum external gate resistor is 5.6 Ω, and a 4.7 kΩ pull-down resistor close to the MOSFET between gate and source terminals is also recommended. Those resistors must have a non-inductive behavior, as well as most surface-mounted devices (SMD).

The recommended buffer to be used as an interface between the CPU and the gate driver is the Fairchild NC7WZ17, which is capable of delivery 24 mA as sink/source output current operating at 3.3 V.

If the buffer between the CPU and the gate driver operates at 5.0 V, 390 Ω resistors should be put in series with the PWM signals along with a 3.3 V zener diode in parallel with the PWM pins. If the shoot-through protection need to be deactivated by 5.0 V pin/supply, a 560 Ω resistor should be put in series with the DT signal along with 3.3 V zener diode in parallel with the DT pin.